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Title: SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS

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SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS

Field of the Invention

The present invention relates generally to integrated circuits, and particularly to a silicon carbide gate field-effect transistor and complementary metal-oxide-semiconductor (CMOS) compatible method of fabrication.

Background of the Invention

Field-effect transistors (FETs) are typically produced using a standard complementary metal-oxide-semiconductor (CMOS) integrated circuit fabrication process. As well known in the art, such a process allows a high degree of integration such that a high circuit density can be obtained with relatively few well-established masking and processing steps. A standard CMOS process is typically used to fabricate FETs that each have a gate electrode that is composed of n-type conductively doped polycrystalline silicon (polysilicon) material.

The intrinsic properties of the polysilicon gate material affects operating characteristics of the FET that is fabricated using a standard CMOS process. Silicon (monocrystalline and polycrystalline) has intrinsic properties that include a relatively small energy band gap (E_g), e.g. approximately 1.2 Volts, and a corresponding electron affinity (χ) that is relatively large, e.g. $\chi \approx 4.2$ eV. For example, for p-channel FETs fabricated by a typical CMOS process, these and other material properties result in a large turn-on threshold voltage (V_T) magnitude. As a result, the V_T magnitude must be downwardly adjusted by doping the channel region that underlies the gate electrode of the FET. Doping to adjust the V_T magnitude typically includes the ion-implantation of acceptor dopants, such as boron, through the polysilicon gate material and an underlying gate insulator into the channel region of the underlying silicon substrate. A typical V_T

magnitude of approximately 0.7 Volts results from the ion-implantation adjustment step.

One drawback of polysilicon gate FETs is that the V_T magnitude adjustment by ion-implantation is particularly difficult to carry out in semiconductor-on-insulator (SOI) and other thin film transistor technology. In SOI technology, the FET channel region is formed in a semiconductor layer that is formed upon an insulating region of the substrate. The semiconductor layer may be only 1000Å thick, making it difficult to obtain a sufficiently sharply defined dopant distribution through ion-implantation.

Another drawback of polysilicon gate FETs is that their intrinsic characteristics are likely to change during subsequent high temperature process steps. For example, the polysilicon gate is typically doped with boron impurities that have a high diffusivity in polysilicon. Because of this high diffusion rate, the boron impurities that are introduced into the polysilicon gate electrode of the FET diffuse through the underlying gate oxide during subsequent high temperature processing steps. As a result, the V_T magnitude the FETs may change during these subsequent high temperature processing steps.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a transistor having an even lower V_T magnitude, in order to operate at lower power supply voltages. There is an additional need in the art to obtain such lower V_T magnitudes without using ion-implantation, particularly for thin film transistor devices in a SOI process. There is a further need in the art to obtain V_T magnitudes that remain stable in spite of subsequent thermal processing steps.

Halvis et al. (U.S. Patent Number 5,369,040) discloses a charge-coupled device (CCD) photodetector which has transparent gate MOS imaging transistors fabricated from polysilicon with the addition of up to 50% carbon, and preferably about 10% carbon, which makes the gate material more transparent to the visible portion of the energy spectrum. However, the Halvis et al. patent is directed to improving gate

transmissivity to allow a greater portion of incident light in the visible spectrum to penetrate the gate. Halvis et al. did not recognize the need to improve the gate characteristics of FETs by lowering V_T magnitudes or stabilizing V_T magnitudes over subsequent thermal processing steps. Halvis et al. does not disclose or suggest the use of carbon in a field-effect transistor gate in the absence of incident light. Thus, the above described needs are unresolved in the art of fabrication of FETs using CMOS processes.

Summary of the Invention

One aspect of the present invention provides a field-effect transistor (FET) having an electrically interconnected gate formed of polycrystalline or microcrystalline silicon carbide (SiC) material. The SiC gate material has a lower electron affinity and a higher work function than a polysilicon gate material. The characteristics of the SiC gate FET include a lower threshold voltage (V_T) magnitude and a lower tunneling barrier voltage as compared to polysilicon gate FETs.

Another aspect of the invention provides a method for fabricating a transistor including an electrically interconnected SiC gate. Source and drain regions are fabricated in a silicon substrate, separated from each other and defining a channel region therebetween. An insulating region is fabricated over the channel region. A SiC gate is fabricated over the insulating region. In one embodiment, SiC gate fabrication includes depositing an SiC layer on the insulating region using low pressure chemical vapor deposition (LPCVD) and etching the SiC material to a desired pattern using a reactive ion etch (RIE) process.

The invention provides numerous advantages. For example, the SiC gate FET provides lower V_T magnitudes, allowing integrated circuit operation at lower power supply voltages. The lower power supply voltage, in turn, provides advantages including lower power consumption and ease in downward scaling of transistor dimensions without unacceptably increasing electric fields. The lower V_T magnitudes also enable higher switching speeds and improved performance. The SiC gate FET also

provides lower V_T magnitudes without adjustment by ion-implantation. This is particularly useful for semiconductor-on-insulator (SOI) and other thin film transistor devices in which an adequately sharply defined dopant distribution is difficult to obtain by ion-implantation V_T adjustment. The SiC gate FET also provides V_T magnitudes that are stable in spite of subsequent thermal processing steps. The SiC gate FET further provides more optimal V_T magnitudes for n-channel FETs (e.g., enhancement rather than depletion mode).

Brief Description of the Drawings

In the drawings, like numerals describe substantially similar components throughout the several views.

FIG. **1** is a cross-sectional view, illustrating generally one embodiment of a transistor according to one aspect of the invention, including a silicon carbide (SiC) gate.

FIG. **2** is a graph, illustrating generally barrier height versus tunneling distance for a SiC gate transistor.

FIGS. **3A-3H** illustrate generally examples of process steps for fabricating n-channel and p-channel SiC gate transistors.

FIG. **4** is a simplified block diagram, illustrating generally one embodiment of a semiconductor memory device incorporating SiC gate transistors.

Detailed Description of the Invention

In the following detailed description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, a specific embodiment in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. This embodiment is described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural and electrical changes may be made without departing from the scope of the present

invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The present invention discloses a field-effect transistor (FET) having gate that is formed of a polycrystalline or microcrystalline silicon carbide (SiC) material, which includes any material that incorporates both silicon and carbon into the gate region of a FET. The SiC gate FET includes characteristics such as, for example, a lower electron affinity and a higher work function than a conventional polycrystalline silicon (polysilicon) gate FET. In one embodiment, the FET gate is electrically interconnected or otherwise driven by an input signal. The SiC gate FET provides lower threshold voltage (V_T) magnitudes, allowing operation at lower power supply voltages. This, in turn, allows lower power consumption, and facilitates the downward scaling of transistor dimensions without increasing electric fields unacceptably. The lower V_T magnitudes also enables higher switching speeds and improved performance. The SiC gate FET also provides lower V_T magnitudes without adjustment by ion-implantation. This is particularly useful for semiconductor-on-insulator (SOI) and other thin film transistor devices in which a sufficiently sharp doping profile is difficult to obtain by ion-implantation. The SiC gate FET also includes V_T magnitudes that are stable in spite of subsequent thermal processing steps. The SiC gate FET further provides more optimal threshold voltage magnitudes for n-channel FETs (e.g., enhancement rather than depletion mode). In another embodiment, the SiC gate FET further provides floating gate transistors having lower tunneling barriers, such as described in Forbes

U.S. patent application serial number 08/790,603 entitled "Flash Memory with Microcrystalline Silicon Carbide Film Floating Gate," which is assigned to the assignee of the present application and which is herein incorporated by reference. This allows faster storage and removal of charge from the floating gates, and is particularly useful for speeding erasing and writing operations in flash electrically erasable and programmable read-only memories (EEPROMs) and other applications.

FIG. **1** is a cross-sectional view illustrating generally, by way of example, one embodiment of a n-channel FET provided by the invention. The FET includes a source region **102**, a drain region **104** and a gate region **106**. In one embodiment, source **102** and drain **104** are fabricated by forming regions of highly doped (n+) regions in a lightly doped (p-) silicon semiconductor substrate **108**. In another embodiment, substrate **108** includes a thin semiconductor surface layer formed on an underlying insulating portion, such as in a SOI or other thin film transistor process technology. Source **102** and drain **104** are separated by a predetermined length in which a channel region **110** is formed.

According to one aspect of the invention, gate **106** is formed of SiC material. The silicon carbide material forming gate **106** is described more generally as Si_xC_{1-x}. In one embodiment, the SiC gate material is approximately stoichiometric, i.e., $x \approx 0.5$. However, other embodiments of the invention could include less carbon, i.e., $x < 0.5$, or more carbon, i.e., $x > 0.5$. For example, but not by way of limitation, one embodiment of the SiC gate material is illustrated by $0.1 < x < 0.5$. Another example embodiment is illustrated by way of example, but not by way of limitation, by $0.4 < x < 0.6$. According to one aspect of the invention, the SiC gate material can include either or both polycrystalline or microcrystalline embodiments of the SiC gate material.

In one embodiment, an insulating layer, such as silicon dioxide (oxide) **114** or other insulating layer, is formed by chemical vapor deposition (CVD). Oxide **114** isolates gate **106** from other layers, such as layer **112**. In another embodiment, gate **106** is oxidized to form at least a portion of oxide **114** to isolate gate **106** from other layers such as layer **112**. In one embodiment, for example, layer **112** is a polysilicon control

gate in a floating gate transistor in an electrically erasable and programmable read-only memory (EEPROM) memory cell. In this embodiment, gate **106** is floating (electrically isolated) for charge storage thereupon, such as by known EEPROM techniques. In another embodiment such as, for example, a driven gate embodiment in which gate **106** is electrically interconnected, layer **112** is, a metal or other conductive interconnection line that is located above gate **106**.

The upper layers, such as layer **112** can be covered with a layer **116** of a suitable insulating material in the conventional manner, such as for isolating and protecting the physical integrity of the underlying features. Gate **106** is isolated from channel **110** by an insulating layer such as thin oxide layer **118**, or any other suitable dielectric material. In one embodiment, thin oxide layer **118** is a gate oxide layer that can be approximately 100 angstroms (Å) thick, such as for conventional FET operation. In another embodiment, such as in a floating gate transistor, thin oxide layer **118** is a tunnel oxide material that can be approximately 50 - 100 Å thick.

The SiC gate **106** has particular advantages over polysilicon gates used in FETs fabricated using a conventional complementary metal-oxide-semiconductor (CMOS) process due to different characteristics of the SiC material. For example, SiC is a wide bandgap semiconductor material with a bandgap energy of about 2.1 eV, in contrast to silicon (monocrystalline or polycrystalline), which has a bandgap energy of about 1.2 eV. Moreover, SiC has an electron affinity of about 3.7 to 3.8 eV, in contrast to silicon, which has an electron affinity of about 4.2 eV. The smaller electron affinity of the SiC gate **106** material reduces the barrier potential at the interface between gate **106** and thin oxide layer **118**. In an embodiment in which thin oxide layer **118** is a tunnel oxide in a floating gate transistor EEPROM memory cell, the lower electron affinity of SiC reduces the tunneling distance and increases the tunneling probability. This speeds the write and erase operations of storing and removing charge by Fowler-Nordheim tunneling to and from the gate **106**, which is a floating gate. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously. The large charge that must be transported by

Fowler-Nordheim tunneling during the erasure of a flash EEPROM typically results in relatively long erasure times. By reducing the tunneling distance and increasing the tunneling probability, the SiC gate **106** reduces erasure times in flash EEPROMs.

P-type SiC also has a larger work function than polysilicon, providing other advantages for a FET having a SiC gate **106**, particularly in an electrically interconnected or driven gate embodiment of the present invention. For example, large work function gates provide advantages for FETs fabricated using SOI starting material and process technology. In an SOI process, p-channel polysilicon gate FETs typically operate as fully depleted thin film transistor devices and require V_T magnitude adjustment by ion-implantation. However, such ion-implantation adjustment is difficult because the semiconductor layer may be only 1000Å thick, making it difficult to obtain a sufficiently sharply defined dopant distribution through ion-implantation. The p-type SiC gate, however, has a larger work function than polysilicon, thereby providing reduced V_T magnitudes for p-channel FETs without adjustment by ion-implantation. The reduced V_T magnitudes of the p-channel FETs advantageously allows operation at lower power supply voltages. This, in turn, lowers power consumption and facilitates the downward scaling of FET dimensions without increasing electric fields unacceptably. The reduced V_T magnitudes also enable higher switching speeds and improved integrated circuit performance. Furthermore, the V_T magnitudes obtained according to the present invention are stable in spite of subsequent thermal processing steps, since no migratory dopants are ion-implanted to adjust the p-channel V_T magnitude. Such lower V_T magnitudes and accompanying advantages are difficult to achieve by other integrated circuit manufacturing techniques.

Large work function p-type SiC gates also provide advantages for n-channel FETs. For example, while polysilicon gate FETs tend to result in depletion mode n-channel V_T magnitudes, p-type SiC gates more easily provide enhancement mode operation, which is often a more desirable device characteristic for designing integrated circuits.

FIG. **2** illustrates generally how the smaller electron affinity provides a smaller barrier potential. The smaller barrier potential reduces the distance that electrons stored on the gate have to traverse by Fowler-Nordheim tunneling to be stored upon or removed from the polycrystalline or microcrystalline SiC gate **106**. The reduced tunneling distance allows easier charge transfer, such as during writing or erasing data in a floating gate transistor in a flash EEPROM memory cell. In FIG. **2**, "do" represents the tunneling distance of a typical polysilicon floating gate transistor due to the barrier height represented by the dashed line "OLD". The tunneling distance "dn" corresponds to a SiC gate and its smaller barrier height represented by the dashed line "NEW". Even a small reduction in the tunneling distance results in a large increase in the tunneling probability, because the tunneling probability is an exponential function of the reciprocal of the tunneling distance. The increased tunneling probability of the SiC gate **106** advantageously provides faster programming and erasure times for SiC gate floating gate transistors in flash EEPROM memories. Flash EEPROM memories using lower V_T magnitude SiC gate floating gate transistors also operate at lower power supply voltages, as described above.

The transistor of FIG. **1** illustrates generally, by way of example, an n-channel FET that includes an SiC gate. In one embodiment, for example, the transistor can be formed on substrate **108** using an n-well CMOS process, enabling monolithic CMOS fabrication of n-channel and p-channel FETs on a common substrate. In one embodiment, both the n-channel and the p-channel FETs include a polycrystalline or microcrystalline SiC gate. Thus, with appropriate doping, the FET illustrated in FIG. 1 could also represent a p-channel FET. Applications of the p-channel and n-channel SiC gate FETs include any application in which conventionally formed polysilicon gate FETs are used.

FIGS. **3A** - **3H** illustrate generally examples of process steps for fabricating n-channel and p-channel SiC gate transistors according to the present invention. The n-channel and p-channel FETs can be produced on a silicon or other semiconductor

substrate, an SOI substrate, or any other suitable substrate **108**. Only the process steps that differ from conventional CMOS process technology are described in detail.

In FIG. **3A**, substrate **108** undergoes conventional CMOS processing up to the formation of the gate structure, including formation of field oxide 300 for defining active regions 302, and the formation of well regions, such as n-well 304 in which p-channel transistors will be fabricated.

In FIG. **3B**, an insulating layer, such as thin oxide layer **118**, is formed on substrate **108**, such as by dry thermal oxidation, including over the portions of the active area regions **302** in which n-channel and p-channel FETs are formed. In one embodiment, thin oxide layer **118** is a gate oxide layer that can be approximately 100 angstroms (Å) thick. In another embodiment, such as in a floating gate transistor, thin oxide layer **118** is a tunnel oxide material that can be approximately 50 - 100 Å thick.

In FIG. **3C**, a thin film **306** of conductively doped polycrystalline or microcrystalline SiC is then deposited, such as by chemical vapor deposition (CVD) over the entire wafer, including over thin oxide layer **118**. The chemical composition of thin film **306** may be different for the particular deposition conditions of the polycrystalline and microcrystalline SiC, as illustrated by way of the particular examples described above.

Conventional FETs usually use n+ doped (e.g., phosphorus as dopant) gate regions for both p-channel and n-channel FETs, even though it p+ doped (e.g., boron as dopant) gate regions would provide more desirable operating characteristics. This is because boron easily diffuses out of the polysilicon gate regions during subsequent high temperature processing steps. By contrast, one aspect of the present invention is that it allows formation of n+ doped or p+ doped SiC gate regions. Since the diffusion rate of the boron dopant is lower in SiC than in polysilicon, boron can be used as a dopant in the SiC gate material. Thus, one advantage of the present invention is that the V_T magnitudes in the SiC gate FETs are less affected by subsequent high temperature process steps than those of conventional polysilicon gate FETs. This allows greater control of the V_T magnitudes in the SiC gate FETs of the present invention.

In one embodiment, for example, SiC film **306** is deposited using low-pressure chemical vapor deposition (LPCVD), providing the structure illustrated in FIG. **3C**. The LPCVD process uses either a hot-wall reactor or a cold-wall reactor with a reactive gas, such as a mixture of $Si(CH_3)_4$ and Ar. Examples of such processes are disclosed in an article by Y. Yamaguchi et al., entitled "Properties of Heteroepitaxial 3C-SiC Films Grown by LPCVD", in the 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Digest of Technical Papers, page 3. vol. (934+1030+85), pages 190-3, Vol. 2, 1995, and in an article by M. Andrieux, et al., entitled "Interface and Adhesion of PECVD SiC Based Films on Metals", in supplement Le Vide Science,Technique et Applications. (France), No. 279, pages 212-214, 1996. However, SiC film **306** can be deposited using other techniques such as, for example, enhanced CVD techniques known to those skilled in the art including low pressure rapid thermal chemical vapor deposition (LP-RTCVD), or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy (MBE). Other examples of forming SiC film **306** include reactive magnetron sputtering, DC plasma discharge, ion-beam assisted deposition, ion-beam synthesis of amorphous SiC films, laser crystallization of amorphous SiC, laser reactive ablation deposition, and epitaxial growth by vacuum anneal. The conductivity of the SiC film **306** can be changed by ion implantation during subsequent process steps, such as during the self-aligned formation of source/drain regions for the n-channel and p-channel FETs.

In FIG. **3D**, SiC film **306** is patterned and etched, together with the underlying thin oxide layer **118**, to form SiC gate **106**. SiC film **306** is patterned using standard techniques and is etched using plasma etching, reactive ion etching (RIE) or a combination of these or other suitable methods. For example, SiC film **306** can be etched by RIE in a distributed cyclotron resonance reactor using a SF_6/O_2 gas mixture using SiO_2 as a mask with a selectivity of 6.5. Such process is known in the art and is disclosed, for example, in an article by F. Lanois, entitled "Angle Etch Control for Silicon Power Devices", which appeared in Applied Physics Letters, Vol 69, No. 2,

pages 236-238, July 1996. Alternatively, SiC film **306** can be etched by RIE using the mixture SF_6 and O_2 and $F_2/Ar/O_2$. An example of such a process is disclosed in an article by N. J. Dartnell, et al., entitled "Reactive Ion Etching of Silicon Carbide" in Vacuum, Vol. 46, No. 4, pages 349-355, 1955. The etch rate of SiC film **306** can be significantly increased by using magnetron enhanced RIE.

FIG. **3E** illustrates one embodiment in which SiC gate **106** is oxidized after formation, providing a thin layer **310** represented by the dashed line in FIG. **3E**. SiC gate **106** can be oxidized, for example, by plasma oxidation similar to reoxidation of polycrystalline silicon. During the oxidation process, the carbon is oxidized as carbon monoxide or carbon dioxide and vaporizes, leaving the thin layer **310** of silicon oxide over SiC gate **106**. In one embodiment, thin layer **310** is used as, or as a portion of, an intergate dielectric between floating and control gates in a floating gate transistor embodiment of the present invention.

FIG. **3F** illustrates generally a self-aligned embodiment of the formation of n-channel FET source/drain regions **312** and p-channel FET source/drain regions **314** for the p-channel FET. The doping of SiC gate **106** can be changed by ion implantation, such as during the formation of n-channel FET source/drain regions **312** or p-channel FET source/drain regions **314** for the p-channel FET. For example, a p-type SiC film **306** can be deposited, and its doping then changed to n+ by leaving SiC gate **106** unmasked during the formation of the n+ source/drain regions **312** for the n-channel FET.

FIG. **3G** illustrates generally the formation of an insulating layer, such as oxide **114** or other suitable insulator, after formation of n-channel FET source/drain regions **312** and p-channel FET source/drain regions **314** for the p-channel FET. In one embodiment, oxide **114** is deposited over the upper surface of the integrated circuit structure using a standard CVD process. Oxide **114** isolates SiC gate **106** from other gates such as, for example, an overlying control gate layer **112** where SiC gate **106** is a floating gate in a floating gate transistor EEPROM memory cell. Oxide **114** also isolates SiC gate **106** from any other conductive layer **112**, such as polysilicon layers,

gates, metal lines, etc., that are fabricated above and over SiC gate **106** during subsequent process steps. Insulating layer **116** is produced on the structure in a conventional manner.

FIG. **4** is a simplified block diagram illustrating generally one embodiment of a memory **400** system incorporating SiC gate FETs according to one aspect of the present invention. The SiC gate FETs are used in various applications within memory **400** including, for example, in logic and output driver circuits. The SiC gate FETs can also function as memory cell access FETs, such as in a dynamic random access memory (DRAM) embodiment of memory **400**, or as other memory elements therein. In one embodiment, memory **400** is a flash EEPROM, and the SiC gate FETs are floating gate transistors that are used for nonvolatile storage of data as charge on the SiC floating gates. However, the SiC gate FETs can also be used in other types of memory systems, including SDRAM, SLDRAM and RDRAM devices, or in programmable logic arrays (PLAs), or in any other application in which transistors are used.

FIG. 4 illustrates, by way of example but not by way of limitation, a flash EEPROM memory **400** comprising a memory array **402** of multiple memory cells. Row decoder **404** and column decoder **406** decode addresses provided on address lines **408** to access addressed SiC gate floating gate transistors in the memory cells in memory array **402**. Command and control circuitry **410** controls the operation of memory **400** in response to control signals received on control lines **416** from a processor **401** or other memory controller during read, write, and erase operations.

As described above, the floating SiC gates of the floating gate transistors in memory array **402** advantageously reduce the tunneling distance and increase the tunneling probabilities, thereby speeding write and erase operations of memory **400**. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously, which normally results in relatively long erasure times. By reducing the tunneling distance and increasing the tunneling probability, charge is more easily transferred to and from the SiC floating gates, thereby reducing erasure times in flash EEPROMs.

Conclusion

Thus, the present invention provides a FET having a polycrystalline or microcrystalline SiC gate. The SiC gate FET characteristics include a lower electron affinity and higher work function than a conventional polysilicon gate FET. The SiC gate FET provides lower V_T magnitudes, allowing operation at lower power supply voltages. This, in turn, lowers power consumption and facilitates downward scaling of transistor dimensions without increasing electric fields unacceptably. The lower V_T magnitudes also enable higher switching speeds and improved performance. The SiC gate FET also provides lower V_T magnitudes without adjustment by ion-implantation. This aspect of the invention is particularly useful for SOI, thin film transistors, and any other devices in which ion-implantation may not yield a sufficiently sharp dopant distribution. The SiC gate FET provides V_T magnitudes that are stable in spite of subsequent thermal processing steps. The SiC gate FET also provides more optimal threshold voltage magnitudes for n-channel FETs (e.g., enhancement rather than depletion mode). In one embodiment, the SiC gate FET has an electrically interconnected or driven gate. In another embodiment, the SiC gate FET further provides floating gate transistors that allow faster storage and erasure such as, for example, used in flash EEPROMs.

Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

WHAT IS CLAIMED IS:

1. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected gate formed of a silicon carbide material.

2. The transistor of claim **1**, wherein the gate comprises polycrystalline silicon carbide.

3. The transistor of claim **1**, wherein the gate comprises microcrystalline silicon carbide.

4. The transistor of claim **1**, wherein the transistor is a p-channel device.

5. The transistor of claim **1**, wherein the transistor is an n-channel device.

6. The transistor of claim **1**, wherein the silicon carbide gate material is described by $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5

7. The transistor of claim **6**, wherein X is approximately equal to 0.5.

8. The transistor of claim **1**, wherein the gate is separated from the channel by an insulating layer.

9. The transistor of claim **8**, wherein the insulating layer is approximately between 50 angstroms and 100 angstroms thick.

10. The transistor of claim **8**, wherein the insulating layer is approximately 100 angstroms thick.

11. An integrated circuit device comprising:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer.

12. The integrated circuit device of claim **11**, wherein the p-channel and n-channel silicon carbide gates comprise polycrystalline silicon carbide.

13. The integrated circuit device of claim **11**, wherein the p-channel and n-channel silicon carbide gates comprise microcrystalline silicon carbide.

14. The integrated circuit device of claim **11**, wherein the insulating layers, which separate the silicon carbide gates in each of the n-channel and p-channel transistors from their respective channel regions, are comprised of silicon oxide.

15. A semiconductor memory device comprising:

a memory array including a plurality of transistors, at least one of the transistors including an electrically interconnected gate formed of a silicon carbide material;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

16. A method of fabricating a transistor, the method comprising the steps of:

fabricating source and drain regions in a substrate, a separation between the source and drain regions defining a channel region;

fabricating an insulating layer overlying the channel region; and

fabricating an electrically interconnected silicon carbide gate on the insulating layer.

17. The method of claim **16**, wherein fabricating the silicon carbide gate includes the steps of :

depositing a layer of silicon carbide material on the insulating region using low pressure chemical vapor deposition; and

etching the silicon carbide material to a desired pattern using a reactive ion etch process.

18. The method of claim **17**, wherein etching the silicon carbide material further includes using plasma etching in combination with the reactive ion etching.

20. The method of claim **18**, further comprising the step of oxidizing the silicon carbide material to form a thin layer of oxide on the silicon carbide material.

21. The method of claim **17**, wherein the insulating region has a thickness of approximately 100 angstroms.

22. The method of claim **17**, wherein the insulating region has a thickness of approximately between 50 angstroms and 100 angstroms.

SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS

Abstract of the Disclosure

A field-effect transistor (FET) device and method of fabrication uses an electrically interconnected polycrystalline or microcrystalline silicon carbide (SiC) gate having a lower electron affinity and higher work function than a polysilicon gate FET. The smaller threshold voltage magnitude of the SiC gate FET allows reduced power supply voltages (lowering power consumption and facilitating downward scaling of transistor dimensions), and enables higher switching speeds and improved performance. The smaller threshold voltage magnitudes are obtained without ion-implantation, which is particularly useful for SOI and thin film transistor devices. Threshold voltage magnitudes are stable in spite of subsequent thermal processing steps. N-channel threshold voltages are optimized for enhancement mode.

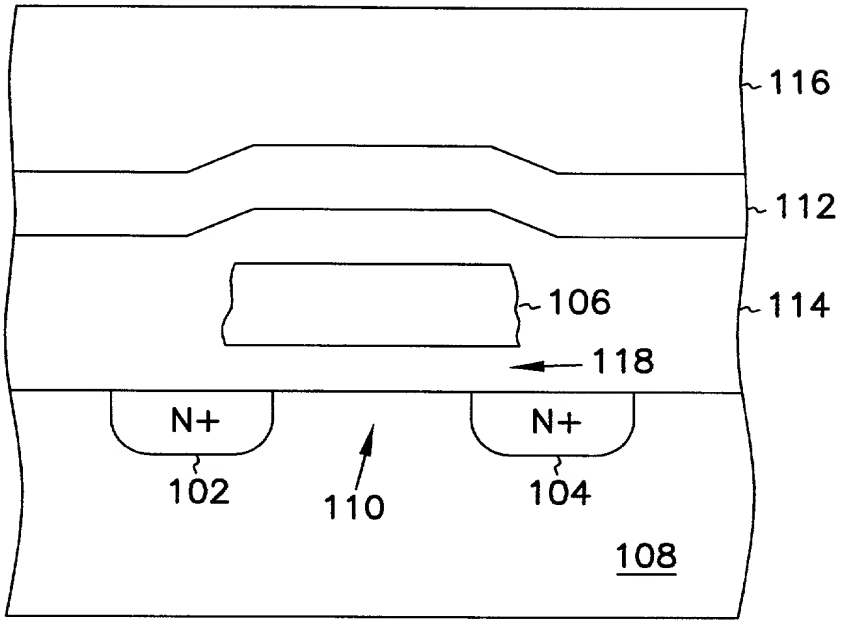

116
112
106
114
118
N+
N+
102
110
104
108

FIG. 1

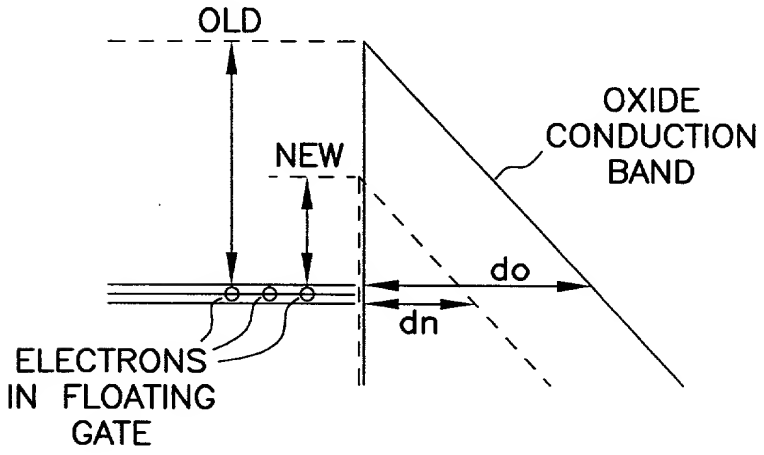

OLD
NEW
OXIDE
CONDUCTION
BAND
do
dn
ELECTRONS
IN FLOATING
GATE

FIG.2

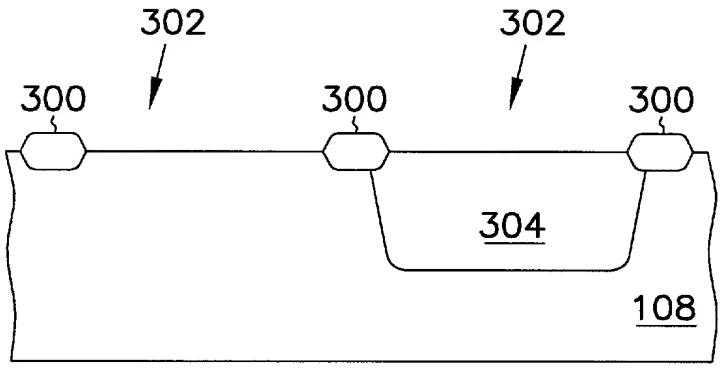


FIG. 3A

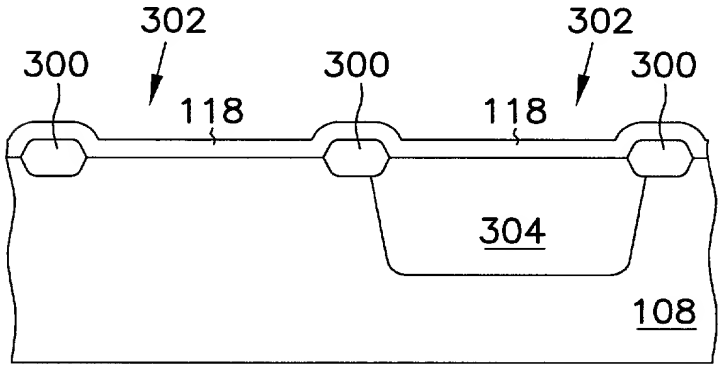


FIG. 3B

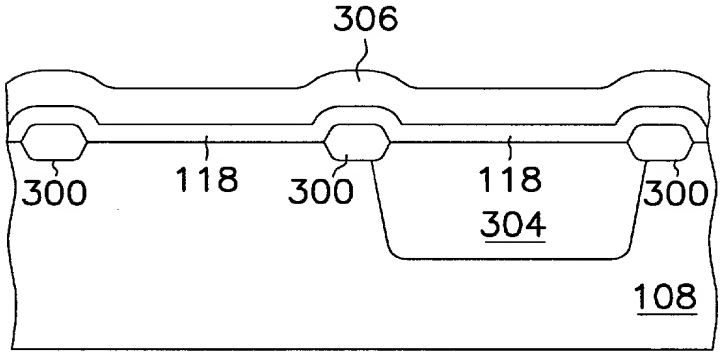


FIG. 3C

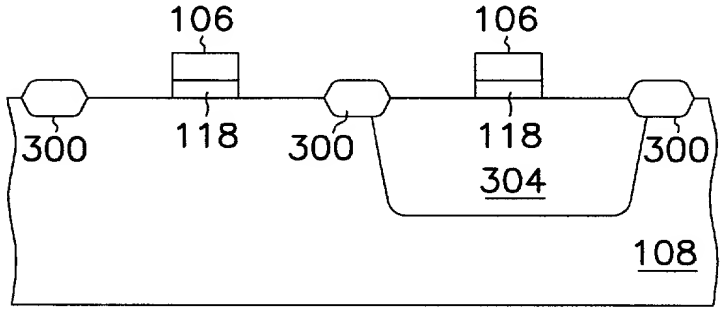


FIG. 3D

FIG. 3E

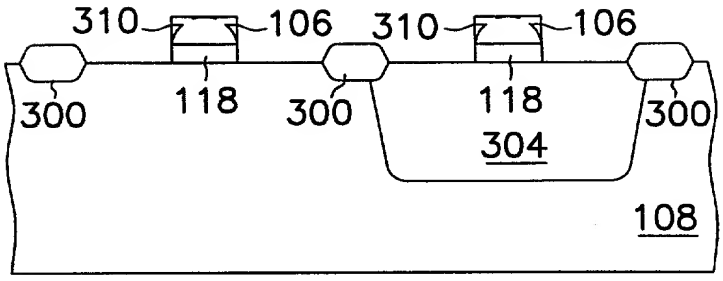


FIG. 3F

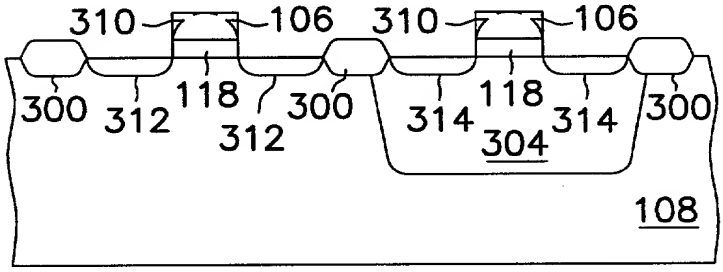


FIG. 3G

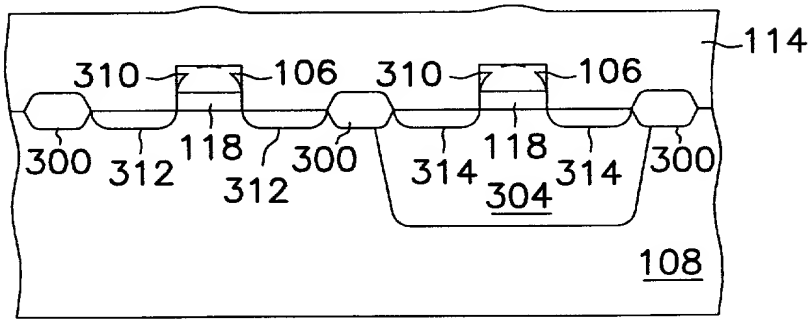
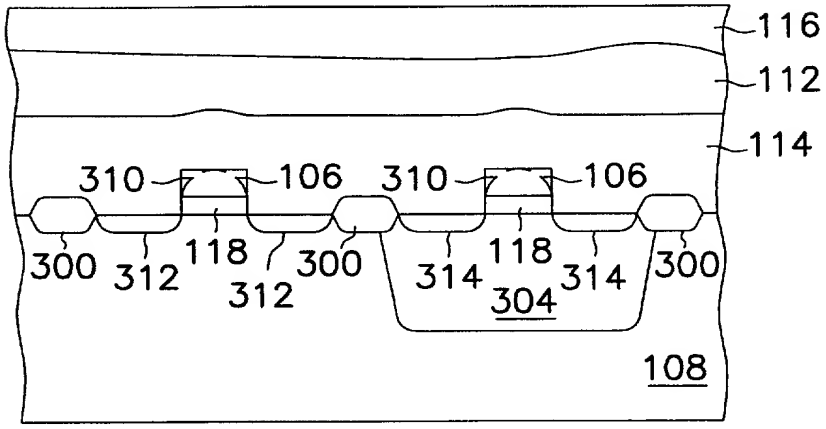


FIG. 3H



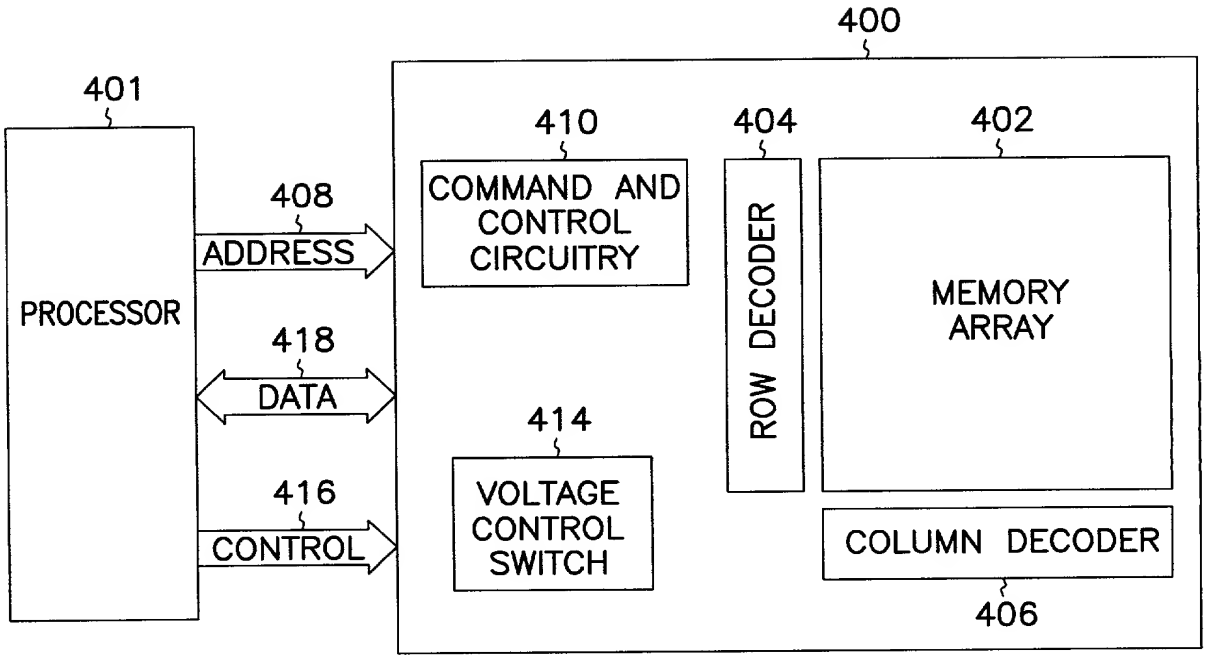

400
401
PROCESSOR
408
ADDRESS
418
DATA
416
CONTROL
410
COMMAND AND CONTROL CIRCUITRY
414
VOLTAGE CONTROL SWITCH
404
ROW DECODER
402
MEMORY ARRAY
COLUMN DECODER
406

FIG. 4

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billig, Patrick G.	Reg. No. 38,080	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Billion, Richard E.	Reg. No. 32,836	Harris, Robert J.	Reg. No. 37,346	Pappas, Lia M.	Reg. No. 34,095
Brennan, Thomas F.	Reg. No. 35,075	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Klima-Silberg, Catherine I.	Reg. No. 40,052	Slifer, Russell D.	Reg. No. 39,838
Dryja, Michael A.	Reg. No. 39,662	Kluth, Daniel J.	Reg. No. 32,146	Viksnins, Ann S.	Reg. No. 37,748
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198	Woessner, Warren D.	Reg. No. 30,440
Farney, W. Bryan	Reg. No. 32,651	Litman, Mark A.	Reg. No. 26,390		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/ firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: June 18, 1997
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

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(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

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Signature: _____ Date: 17 June 97
Leonard Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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